FORM PTO-1083

Case Docket No. PD-8811

In re Application of Michio Asahina
Serial No. 07/780,455

Date: November 25, 1992

Filed: October 22, 1991

For: SEMICONDUCTOR DEVICE

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment/response in the above-identified application.

___ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.
___ A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.
X No additional fee is required.
___ Information Disclosure Statement

The fee has been calculated as shown below:

	(Col. 1) CLAIMS REMAINING AFTER AMENDMENT		(Col. 2) HIGHEST NO. PREVIOUSLY PAID FOR		(Col. 3) PRESENT EXTRA	SMALL ENTITY RATE	ADDIT. FEE	OR	OTHER THAN A SMALL ENTITY RATE	ADDIT. FEE
TOTAL	* 4	MINUS	** 24	=	0	x11	$	OR	x22	$
INDEP CLAIMS	* 3	MINUS	*** 4	=	0	x37	$	OR	x74	$
___ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM						+115	$	OR	+230	$
					TOTAL		$	OR	TOTAL	$ 0

* If the entry in Col. 1 is less than the entry in Col. 2. write "O" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box on Col. 1 of a prior amendment or the number of claims originally filed.

___ Please charge my Deposit Account No. 19-3725 the amount of $_____. A duplicate copy of this sheet is enclosed.

___ A check in the amount of $_____ to cover the extension fee is enclosed.

___ A check in the amount of $_____ to cover the filing fee is enclosed.

___ A check in the amount of $200.00 to cover the Information Disclosure Statement.

___ A check in the amount of $130.00 to cover the Information Disclosure Statement.

X The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 19-3725. A duplicate copy of this sheet is enclosed.
X Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
X Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

Jay M. Finkelstein, 21,082

SPENSLEY HORN JUBAS & LUBITZ
ATTORNEYS AT LAW
1880 CENTURY PARK EAST, FIFTH FLOOR
LOS ANGELES, CALIFORNIA 90067
(310) 553-5050

PATENT
PD-8811FWC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
MICHIO ASAHINA
Serial No.: 07/780,455
Filing Date: October 22, 1991
For: SEMICONDUCTOR DEVICE

ART GROUP UNIT: 2508
EXAMINER: S. Loke

AMENDMENT

Honorable Commissioner of
Patents & Trademarks
Washington, D.C. 20231

Dear Sir:

In response to the Examiner's Action dated August 26, 1992, kindly amend the above-identified application as follows:

IN THE CLAIMS:

Kindly cancel claims 1-24 and add new claims 25-28 as follows:

-- 25. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region and a gate wiring, forming a lower conductor structure, and forming an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein each said step of forming a conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film; and

performing a plating operation in order to form a metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer.

26. A method as defined in claim 25 wherein the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

27. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region, a gate wiring, a lower conductor structure, and an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein said step of forming an upper conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film;

performing a plating operation in order to form a metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer; and

after said step of performing a plating operation, performing a thermal treatment in order to diffuse material from the plating layer into the at least one layer.

28. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region, a gate wiring, and an insulating layer overlying said semiconductor region and having at least one through opening; and

forming a conductor structure on the insulating layer and causing the conductor structure to extend into the through opening;

wherein said step of forming a conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film;

forming a patterned resist layer on the at least one conductor layer, the patterned resist layer having at least one opening which exposes a part of the at least one conductor layer;

performing a plating operation in order to form a metal plating layer on the at least one conductor layer in the opening in the patterned resist layer, so that the metal plating layer adheres to the at least one conductor layer;

removing the patterned resist layer; and

removing portions of the at least one conductor layer which are not covered by the metal plating layer, by an etching operation, using the metal plating layer as an etching mask.

REMARKS

The Examiner's Action dated August 26, 1992, has been received, and its contents carefully noted. In addition, receipt is acknowledged, with appreciation, of the Examiner Interview Summary Record dated September 15, 1992, in which the Examiner confirms that the office action of August 26, 1992 does not present a final rejection.

In order to advance prosecution, the previously pending claims have been cancelled and replaced by new method claims 25-28. These claims have been drafted to define the contribution of the invention over the prior art with greater particularity.

Claim 25 distinguishes over the prior art in that it specifies that both the lower conductor structure and the upper conductor structure is formed from at least one layer and a metal plating layer which is formed on, and adheres to, the at least one layer. By this method, the advantages offered by the conductor structure fabrication method according to the invention, relating particularly to elimination of stress migration and electro migration, as well as voids and projections in the conductor structures, can be fully realized. It will be noted that in the method defined in claim 25 the lower conductor structure, which is covered with an insulating layer, is formed in the manner described above. One significant result is that projections, such as shown at 1116 in Fig. 2(b) will not grow on the lower conductor structure during subsequent heating processes. These projections promote current leakage between insulating layers. Specification, page 5, lines 1-4.

In the method described at column 10, lines 13-65 of Del Monte, a contact electrode bump 23 is formed by electroplating. It also appears possible that a gold flash layer 21 is formed by electroplating. However, this is not completely certain since the

thin gold flash layer is sputtered on the entire surface of the wafer." Lines 9-10. It is well recognized in the art that sputtering is a process which is quite different from electroplating. In any event, this reference only discloses plating associated with forming an electrode bump and there is no disclosure of forming an insulating layer over a plated layer or of subsequently subjecting the device to a heat treatment which would result in the creation of projections. In more general terms, there is no disclosure in this reference that any advantage would be served by forming conductor structures with a plating layer when those conductor structures are at least partially separated by an insulating layer.

In further accordance with the disclosure of this reference, the layer on which the layer 17-23 is formed is identified simply as an interconnection network made of aluminum. Column 6, lines 32-39. There is nothing in the disclosure of this reference which would suggest to one skilled in the art any particular method for fabricating the interconnection network 11.

The primary reference, McDavid, does not disclose a device including a lower conductor structure and an upper conductor structure, with the upper conductor structure being connected to the lower conductor structure.

Thus, no reasonable combination of the teachings of the applied references can be considered to suggest the method now defined in claim 25.

Claim 26 further defines patentably over the applied references by its recitation that the at least one layer of the upper conductor structure contact the metal plating layer of the lower conductor structure.

Claim 27 defines patentably over the prior art by its recitation that the step of forming an upper conductor structure

treatment in order to diffuse material from the plating layer into the at least one layer. Such a step is not disclosed in either of the applied references. As described at page 12, lines 11-15 of the present specification, the plating operation in combination with the thermal treatment results in a device in which the projections 1116 depicted in Figures 1 and 2 are entirely avoided.

Claim 28 is directed to a novel embodiment of the invention, one example of which is illustrated in Figures 5d and e of the application drawing, according to which the metal plating layer is deposited in openings formed in a patterned resist layer, after which the resist layer is removed and portions of the conductor layer underlying the plating layer are removed by etching, using the plating layer as a mask. This method is described in the specification, particularly at page 16. This represents an efficient method for giving the conductor structure a well defined configuration. A particular advantage is that the plating layer performs the dual function of improving the performance characteristics of the conductor structure and serving as an etching mask. The outline of the resulting conductor structure is well defined in view of the inherent ability of plating to form a uniform layer which completely fills an opening in a plating mask.

The method defined in claim 28 is not disclosed in or suggested by the applied references.

Accordingly, it is believed that the claims now in the application define methods which bear no relation to those disclosed in the applied references, and therefore define patentably thereover. It is therefore requested that the rejections of record be reconsidered and withdrawn and that the application be allowed.

If for any reason, the Examiner finds the application in other than a condition for allowance, he is respectfully requested to call the undersigned attorney at the Washington, D.C. telephone number 223-5700 to discuss the steps necessary for placing the application in condition for allowance.

11/25/92
Date

Respectfully submitted,

Jay M. Finkelstein, 21,082

SPENSLEY HORN JUBAS & LUBITZ
1880 Century Park East, Ste. 500
Los Angeles, California 90067
(213) 553-5050
(202) 223-5700

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on November 25, 1992.

Jay M. Finkelstein, Reg. No. 21,082

(signature) 11/25/92 (date)

RECEIVED
SEP 18 1992
FOREIGN FILING
NAME:

Spiro Papov

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/780,493	10/22/91	ASAHINA M	PD-881EMC

SPENSLEY HORN JUBAS & LUBITZ
1880 CENTURY PARK EAST, STE. 500
LOS ANGELES, CA 90067

EXAMINER	
TSAI, H	
ART UNIT	PAPER NUMBER
1107	34

DATE MAILED:

EXAMINER INTERVIEW SUMMARY RECORD

09/15/92

All participants (applicant, applicant's representative, PTO personnel):

(1) Mr. Jay Finkelstein (3) _____

(2) H Jey Tsai (4) _____

Date of Interview 9/15/92

Type: ☑ Telephonic ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☑ No. If yes, brief description: _____

Agreement ☑ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: 23

Identification of prior art discussed: None

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

(a) The Restriction was made final not office Action on 6/6/92

(b) The box "this action is made final" in Cover page of office Action Paper #32 was inadvertantly Marked and therefore is withdrawn.

Applicant response is due on 11/27/92

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

Unless the paragraphs below have been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW (e.g., items 1 – 7 on the reverse side of this form). If a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☑ It is not necessary for applicant to provide a separate record of the substance of the interview.

☐ Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action.

Examiner's Signature

PTOL-413 (REV. 1-84)

APPLICANT'S COPY